Example DDR
Test Configurations
Example DDR test configuration for a desktop computer platform

Memtest utility generating read-write test output (random number sequence)

- Clock
- Strobe
- Data
- Waveforms acquired on scope

Probes soldered to Clock, Strobe, and Data lines

Probe tips soldered and hot glued to vias on DIMM
Example DDR test configuration for a netbook computer

Solder-In Probes Tips
Connected to Clock, Strobe, and Data Lines of the DDR SODIMM on an ASUS Netbook

Differential Clock Line – Probe leads soldered to two vias directly opposite the differential termination on the other side of the board.

Single-ended Data Line – Probe leads soldered to the memory "chip side" of the series resistor array and ground.

Differential Strobe Line – Probe leads soldered to the memory "chip side" of the series resistor array.
Best Practices for DDR Probing
Recommended DDR probing method 1: Hands-free probe holder mounted in reverse position
Strain relief for the probing connection can be provided by utilizing this counter-weight configuration

The typical use model for a hands-free probe holder is designed to place weight at the tip of the probe

Not recommended probing configuration for DDR

Recommended probing configuration for DDR

This reverse mount acts as a counterweight, removing force from the probe tip, and providing strain relief for the probing connection during DDR testing
Recommended DDR Probing Method 2: Gooseneck strain relief

Mount adhesive base on nearby chip, strain relief is provided to the solder tips

A probe with flat geometry and rubberized flex circuit lead can be easily secured in place.
Recommended DDR Probing Method 3: Chip clip secures probe to board or chassis

A chip clip prevents movement of the probe platform cable assembly when mounted on a board edge or chassis.

- Chip clip mounted on corner of DDR board
- Chip clip mounted on edge of computer chassis
Best practices example: using Kapton tape and signal labels on the board

- Kapton tape is recommended on the probe interconnect lead (but not the probe flex circuit tip or damping resistor leads).
- Signal labels on the board are recommended.
Tips are soldered to DDR test points.

Best practices example: Gooseneck strain relief is used to prevent movement of probe head.

Gooseneck strain relief protects solder tips while probing strobe and data lines.
Best practices example: using a chip clip, two probe holders, and two gooseneck strain reliefs

Shown below is a combination use of a chip clip, two reverse-mounted hands-free probe holders, and two gooseneck strain reliefs while probing DDR Clock, Strobe, and Data.
Probe leads are taped to the board at two different locations to provide secure strain relief.

An ESD bag is placed under the DDR DUT for static protection. The use of an ESD bag is always recommended, especially when the device is contained on a metal cart.

Although it would be ideal to not move the device under test -- if it must be moved -- using a cart is recommended. The cart provides support for the three probe platform cable assemblies. This configuration could also be improved by anchoring the probe platform cable assembly to the cart with plastic ties, clips, or tape.

Adhesive signal labels are placed on probe tips. Since the probe amplifiers will be disconnected during transport, the labels allow for rapid reconnection by the operator. Labeling could be further improved by adding adhesive labels to the probing points also.
Best practices example: tape has completely secured the probing area for shipping.

Kapton tape is recommended on the probe interconnect leads (but not the probe flex circuit tips or damping resistor leads).

After soldering, the probe tips are completely immobilized in tape, protecting the solder connections from all outside impact.

This amount of taping is recommended if the setup needs to be shipped from one location to another, to ensure that the solder-in leads are firmly secured and the electrical connections remain intact.
Example DDR4 Test Configuration

DDR4 DIMM mounted in slot in computer chassis

Probes leads pre-taped to DDR4 DIMM
Probe leads soldered and taped to DDR4 DIMM before inserting into slot
DDR probe heads hot glued to the back of a single-sided DIMM

Probe tips hot glued to the back side of the BGA ball out of this single-sided DIMM. This allows for secure connections during card insertion into the DDR slot.

Note: always hot glue the top, not the bottom of the probes.
Testing tip: perform test evaluations using single-sided DIMMs when available

Single-sided DIMMs provide fairly easy access to probing on the back side of the BGA. Probing the back side of a DIMM is preferred, as reflections are minimized. When given a choice, a single-sided DIMM is always better than dual-sided, because access to the BGA ball out provides the best signal integrity for the probing connection. For evaluation and testing purposes, single-sided DIMMs provide the easiest path to signal integrity.

However, since most DIMMs are dual-sided with DRAM chips on both sides, the access to vias on the back side of the chip is not always available and an interposer is often needed.
DDR Connectivity with An Interposer
Interposer Connectivity:

Chip interposers are designed for probing extremely close to memory components, and are essential when probing points are otherwise inaccessible.

Side View

- Standard DDR3 socket on interposer, ready for memory component insertion. Also available without this socket.
- Component interposer socket w/posts
- Memory component interposer. Balls on the bottom simply push into the custom socket on the target.
- DIMM or Target
- Solder added to mechanically retain the adapter to the custom socket

Top View

- Chip with interposer
- Chip Without interposer
- An interposer can be most useful in embedded applications and applications where there are chips on both sides of the DIMM
- Interposer Without Chip

The interposer is installed by soldering the bottom side of the interposer to the DDR BGA footprint on the target where the memory component would normally be soldered. The memory component is then soldered to the top side of the interposer.
Another example of SI probes soldered to Clk, DQS, and DQ using a DDR chip interposer.

A DDR chip interposer mounts between the chip and target, or between the chip and DIMM.
View of entire board containing the same interposer
Example of SI probes soldered to Clk, DQS, and DQ using a DDR Interposer

Two interposers mounted, one not currently being used

Clock, Strobe, and Data probed using a DDR chip interposer
Example of using a DDR chip interposer on a device with many serial interfaces including DDR3, HDMI, Ethernet, USB, and others
Example of SI probes soldered to Clk, DQS, and DQ on a DDR Interposer mounted near the edge of a board.
Best practices: use tweezers to manipulate SI probe tips when soldering.

Tweezers are more nimble and provide better placement and accuracy during the soldering process.
DDR4 interposer example
DDR4 interposer example
Probes soldered to Clock, Strobe, and 7 different Data lines

Best practices: solder in advance, extra SI tips to test multiple data lines

9 probe tips are soldered directly to the interposer. Any of the data lines with a probe tip attached can be connected to the amplifier during testing.
Probe LED indicates channel (Yellow = CK, Pink = Strobe, Blue = Data)

Method to keep signals organized
Removing Resistors When Using Interposers
Should damping resistors be removed from solder-in probes when using an interposer?

If the damping resistors are removed from the probe when using an interposer -- the probes terminate into the interposer without damping resistors -- this results in slightly better signal fidelity when connected to the interposer but this also brings disadvantages. Below are the pros and cons associated with removing the resistors.

**Pros:**
- AC response accuracy improvement (3%)
- DC gain accuracy improvement (4%)

**Cons:**
- Need to modify the probe: old leads and resistors removed, replaced with new leads
- The probes cannot be used for other applications or for general purpose use until the resistors and leads are reattached to the probe tip PCB

**Notes:**
- Most users do not remove the resistors.
- If the resistors are removed, the leads should be replaced with 34 gauge wire extending 3mm the probe tip PCB edge
Generating DDR Traffic
Programs which communicate with DIMMs, such as Memtest86, are widely available. The recommended output is Test 7 in Memtest86 which continuously outputs R/W bursts for the duration of the test. A read or write burst should occur at least once per 10 us for compliance testing, but much higher density is recommended. The higher the burst density, the more statistical results can be computed during a DDR compliance test.
Additional DDR Transition Density Examples

![Waveform Examples]

- **Excellent**
- **Bad**
- **OK**
DDR Debug Examples
Mask Failure Locator

Locate the specific UI where a mask failure occurred
Failing Rising Edge vs a Nominal Edge

Zoom of a nominal rising edge

Zoom of failing rising edge

Non-monotonic edge is causing the failing mask hit
Locating Statistical Events with Measurement Zoom

Built-in measurements to qualify the rise times

Zoom to Min, Max, First, Last
DDR Debugging - Trend and Histogram Vref
Trending voltage and timing parameters over thousands of acquisitions
Real-World DDR Debug: Missing Clock Cycles
Debug Steps: Triggering on the Strobe shows unstable (bimodal) clock timing
Debug Steps: Parameter Track of Skew Identifies Anomalies
Debug Steps: Parameter Track Locates Missing Clock Cycles
Real-World DDR Debug: Logic Problems, Soldering Problems and Power Supply Noise
Real-World Debug: Logic Levels on DQ inconsistent
Real-World Debug: Power Supply Noise coupled into DQ
Real-World Debug: DDR4 Data Probe soldered to wrong node

Data probe leads had been soldered between DQ1 and DQ5 instead of between DQ0 and ground.
Data probe positive lead soldered to DQ0, with negative lead floating instead of soldered to GND.
Debug Tip: DDR Cycle and Edge Measurements
Multiple-Scenario DDR Eye Patterns and Jitter
DDR Eye Mask Testing

Mask testing using a DDR standard or custom mask can show mask failures due to jitter, reflection, glitches, runts, intersymbol interference, non-monotonic edges, crosstalk, slow rise or fall times, overshoot, noise, and more.
Data and strobe bursts are sorted and arranged to display all acquired Read and Write UIs as separate scenarios.

Overlaying eyes allows valuable skew and timing information.

Clock and Strobe can each be the timing reference.
Parameter Measurements on the DDR Eye
DDR Jitter Analysis with Tj / Rj / Dj jitter breakdown, DCD, Pkpk, RMS, TIE Track and Histogram, BTub Curve, CDF, etc can quantify and identify sources of jitter.
Debugging with DDR Specific Parameters with Statistics
Debugging DDR With Analysis on Isolated Portions of Burst

Data and Strobe on Read eye showing only the first bit after the preamble

Data and Strobe on Write eye showing ignoring the first bit after the preamble
DDR Virtual Probing
Virtual Probing

In DDR systems, access to probe points is limited. Ideally, probe should occur at the ballout of the DRAM. In practice the probe is often required to be over an inch away.
DDR Virtual Probing

Since the probe is not directly attached to the receiver we see the superposition of the incident signal and reflected signal.

The distance from the probing point to the receiver can be measured by using the signal edge like a TDR. It will be \( \frac{1}{2} \) the measured time delay.

\[ \Delta X = 800 \, \text{ps} \]
This LP-DDR2 signal shows significant reflections impacting the signal shape. It is not possible to make accurate measurements on a signal like this. The reflections are due to non-ideal probe placement. The reflections must be removed before proceeding to characterize the signal.
DDR Virtual Probing

Virtual Probe at Receiver
- Quickly compensates for reflections due to imperfect receiver termination
- Does not require S-parameters (S-parameters can be used with Eye Dr II or VirtualProbe)
- Uses familiar termination model
- Effective work-around for probe access challenges on DDR systems
Virtually probed signal:
Reflections removed

Original raw signal:
Reflections present

Virtual probe at receiver settings
Testing Strategy – Virtual Probe

- Virtually move probe location to BGA
- Remove any effects of the interposer or channel through de-embedding
Testing Strategy – Virtual Probe at Receiver (VP@Rcvr)

- Often s-parameters files are not easily obtained for entire channel
- Model the circuit to reduce reflections in the signals under test
Virtual Probe and VP@rcv Setup Examples

VP@rcv setup example

Virtual Probe setup example
Testing Strategy – VP@Rcvr Example

Reflections at Vref have been removed
Testing Strategy – VP@Rcvr Example

Virtually Probing at the receiver dramatically improved the eye
DDR Compliance Testing
Automated DDR Compliance Testing Provides Highest Confidence In Less Time

- Performs each measurement in accordance with the JEDEC standard
- Compares each measured value to the specified limits
- Easily document worst-case results and all statistical information
- Connection diagrams guide user through each test setup
- Stop on test for easy debugging
Instant Accumulation of results, worst-case scenario identified and reported

**Summary Table**

<table>
<thead>
<tr>
<th>Measure</th>
<th>Value</th>
<th>Current Value</th>
<th>Test Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>rCur</td>
<td>3.68 ns</td>
<td>353 ps</td>
<td>Informational Only</td>
</tr>
<tr>
<td>IDDDQS</td>
<td>3.8004 V</td>
<td>347.1816 ps</td>
<td>Informational Only</td>
</tr>
<tr>
<td>VDDQ</td>
<td>5.06 V</td>
<td>307.8516 ps</td>
<td>Informational Only</td>
</tr>
<tr>
<td>sdev</td>
<td>372.8 ps</td>
<td>524</td>
<td>Informational Only</td>
</tr>
</tbody>
</table>

**Overall result:** Pass

**Test Electrical - SlewR of CK**

Timestamp: 11/12/2013 16:19:55
Automatically Generated Compliance Reports

- Report contains:
  - Test values
  - Specified test limits
  - Screen captures

- Can be created as:
  - HTML
  - PDF
Wizard Compliance Feedback Example

- Occurs when less than 10 R/W burst acquired
- Warning depends on which tests are selected

WARNING: Not enough write bursts acquired (0 write bursts).
1) Check that you have captured enough transitions on DQS and DQ.
2) Refine deskew between DQS and DQ until these signals are centered.
Do you want to continue the test?

WARNING: Not enough read bursts acquired (0 read bursts).
1) Check that you have captured enough transitions on DQS and DQ.
2) Refine deskew between DQS and DQ until these signals are aligned.
Do you want to continue the test?
## DDR Compliance Example Measurements

### Clock Tests
- **tCK(avg)** – Average Clock Period
- **tCH(avg)** – Average High Pulse Width
- **tCL(avg)** – Average Low Pulse Width
- **tCK (abs)** – Absolute Clock Period
- **tCH(abs)** – Absolute High Pulse Width
- **tCL(abs)** – Absolute Low Pulse Width
- **tJIT(duty)** – Half Period Jitter
- **tJIT(per)** – Clock Period Jitter
- **tJIT(cc)** – Cycle to Cycle Period Jitter
- **tERR(n per)** – Cumulative error

### Electrical Tests
- **SlewR** – Input Rising Edge Slew Rate
- **SlewF** – Input Falling Edge Slew Rate
- **VIH(ac)** – AC Input Logic High
- **VIH(dc)** – DC Input Logic High
- **VIL(ac)** – AC Input Logic Low
- **VIL(dc)** – DC Input Logic Low
- **VSWING** – Input Signal Maximum
- **SoutR** – Output Slew Rate Rise
- **SoutF** – Output Slew Rate Fall
- **tSLMR** – Output Slew Rate Matching Ratio
- **AC Overshoot Peak Amplitude**
- **AC Overshoot Area Above VDDQ**
- **AC Undershoot Peak Amplitude**
- **AC Undershoot Area Below VSSQ**
- **VID(ac)** – AC Differential Input Voltage
- **VIX(ac)** – AC Differential Input Cross Point Voltage
- **VOX(ac)** – AC Differential Output Cross Point Voltage

### Timing Tests
- **tHZ(DQ)** – DQ High Impedance Time from CK/CK#
- **tLZ(DQ)** – DQ Low Impedance Time from CK/CK#
- **tLZ(DQS)** – DQS Low Impedance Time from CK/CK#
- **tHP** – CK Half Pulse Width
- **tQHS** – DQ Hold Skew Factor
- **tIQH** – DQ/DQS Output Hold Time from DQS
- **tDQSH** – DQS Input High Pulse Width
- **tDQSL** – DQS Input Low Pulse Width
- **tDSS** – DQS Falling Edge to CK Setup Time
- **tDHS** – DQS Falling Edge Hold Time from CK
- **tWPRE** – Write Preamble
- **tWPST** – Write Postamble
- **tRPRE** – Read Preamble
- **tRPST** – Read Postamble
- **tDQSQ** – Skew between DQS and DQ
- **tDQSS** – DQS Latching Transition to Clock Edge
- **tDQSCK** – DQS Output Access Time from CK/CK#
- **tAC** – DQ Output Access Time from CK/CK#
- **tDS(base)** – DQ and DM Input Setup Time
- **tDH(base)** – DQ and DM Input Hold Time
- **tIS(base)** – Address and Control Input Setup Time
- **tIH(base)** – Address and Control Input Hold Time
- **tDS1(base)** – DQ and DM Input Setup Time (Single-ended Strobe)
- **tDH1(base)** – DQ and DM Input Hold Time (Single-ended Strobe)
- **tDQSQ** – Skew between DQS and DQ
- **tDQSS** – DQS Latching Transition to Clock Edge
- **tDQSCK** – DQS Output Access Time from CK/CK#
- **tAC** – DQ Output Access Time from CK/CK#
- **tDS(base)** – DQ and DM Input Setup Time
- **tDH(base)** – DQ and DM Input Hold Time
- **tIS(base)** – Address and Control Input Setup Time
- **tIH(base)** – Address and Control Input Hold Time
- **tDS1(base)** – DQ and DM Input Setup Time (Single-ended Strobe)
- **tDH1(base)** – DQ and DM Input Hold Time (Single-ended Strobe)

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### Table

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH(ac) Max</td>
<td>1.407 V</td>
<td>x &lt;= 1.900 V</td>
</tr>
<tr>
<td>VIH(ac) Min</td>
<td>1.307 V</td>
<td>x &gt;= 900 mV</td>
</tr>
<tr>
<td>VIH(ac) Max</td>
<td>231 mV</td>
<td>x &lt;= 800 mV</td>
</tr>
<tr>
<td>VIH(ac) Min</td>
<td>142 mV</td>
<td>x &gt;= 400 mV</td>
</tr>
<tr>
<td>IDAC min of DQS</td>
<td>1.342 ns</td>
<td>x &gt;= 175 ps</td>
</tr>
<tr>
<td>IDAC min of DQS</td>
<td>1.376 ns</td>
<td>x &gt;= 175 ps</td>
</tr>
<tr>
<td>IDAC min of DQS</td>
<td>1.354 ns</td>
<td>x &gt;= 175 ps</td>
</tr>
<tr>
<td>IDAC min of DQS</td>
<td>1.378 ns</td>
<td>x &gt;= 175 ps</td>
</tr>
<tr>
<td>IDAC min of DQS</td>
<td>1.332 ns</td>
<td>x &gt;= 175 ps</td>
</tr>
<tr>
<td>IDAC min of DQS</td>
<td>1.296 ns</td>
<td>x &gt;= 175 ps</td>
</tr>
<tr>
<td>DQ Overshoot peak amplitude Max</td>
<td>-93 mV</td>
<td>x &lt;= 400 mV</td>
</tr>
</tbody>
</table>
DDR Specialized Connectivity
Difficult-to-access DDR test points can be reached, and/or measurements can be taken under extreme temperatures using a high temperature long lead probe.

High-temp probe:
90 cm leads, -40 deg C to +105 deg C, 5 GHz bandwidth

High-temp probes inserted into temperature chamber
Multi-Channel Testing: Clock, Strobe, and dozens of Data lines can be simultaneously monitored using multi-channel scopes.

Example: 20 GHz x 16 channels
(Enables monitoring and comparison of Clock, Strobe and 14 Data or Control lines)

Example: 30 GHz x 8 channels
(Enables monitoring and comparison of Clock, Strobe and 6 Data or Control lines)

Example: 13 GHz x 64 channels
(Enables monitoring and comparison of Clock, Strobe and 62 Data or Control lines)
Using a multi-channel scope allows all of the data lines to be viewed simultaneously (up to 80 channels)
Multi-channel high bandwidth DDR debug and failure analysis
Debug work on address lines from the register buffer spec, testing returned DIMMs
DDR Probe Deskew
Equipment for DDR Probe Deskew

- Three complete probe systems
- Torque wrench
- Spare solder-in tip
- SMA 50-ohm termination
- Characterization Fixture
- Oscilloscope
Since the three (or four) probe tips will likely already be soldered to the device under test, a fourth (or fifth) probe tip will be used for deskewing.

Three probe tips are already soldered to Clock, Strobe, and Data.

A spare probe tip, used for deskewing all (3 or 4) other probes.
Safety Note About Connecting/Disconnecting Active Probe Components While Powered

- Probe platform/cable assembly can be disconnected from scope anytime while powered.
- Probe tip can be disconnected from probe amplifier anytime during operation (ok to hot-swap).
- Probe amplifier should not be connected or disconnected from probe platform/cable assembly while powered (toggle power off or disconnect probe platform/cable assembly from scope first).
- Probe leads can be disconnected from DUT anytime during operation.
Using a probe characterization fixture attached to the fast edge output of an oscilloscope, the probed signal delay can be directly compared to a known reference while triggering internally on the same edge, allowing precise deskew measurements of all channels without requiring a power splitter.

- SMA 50-ohm termination torqued to PCF
- PCF torqued to fast edge
- Probe tip leads clamped to PCF.
Strain Relief Techniques for Probes During Deskew Process

Additional strain relief for the probe tip can be provided while deskewing by reverse-mounting the platform cable assembly using the hands-free probe holder, or by placing it on a surface near the PCF-200.
Deskew Summary

Measure the fast edge delay through each probe system, and adjust the skew value in the channel menu. Deskew values will be retained during the compliance process.

Steps for deskewing D610 and D620 probes for DDR2/DDR3

Pre-steps:
1. Let the probes warm up for 10-15 minutes.
2. Autozero each probe using the channel menu.
3. Set the Vertical Scaling for all input channels to 100 mV/div.
4. Set the Vertical Offset for all input channels to 0 V.
5. Connect PCF to Fast Edge out as shown in Figure 1.
6. Attach one (any) of the probe tips to the PCF200. The same tip will be used to deskew all (3 or 4) probes.
7a. Terminate the PCF200 using a 50-ohm coaxial connector [shown in Figure 1]
7b. If a coaxial 50-ohm termination is not available, then connect a cable instead [shown in Figure 2] and terminate it into an unused channel (where the channel coupling is set to 50 ohms). Note: Do not use Aux Out to terminate the the cable.

Steps for deskewing:
1. Set the Trigger Source to “FastEdge” in the Trigger menu.
2. Turn on only C1.
3. Connect the C1 probe amplifier and base-cable assembly to the probe tip which is currently attached to the PCF200 (see hot-swapping safety information in Figure 3)
4. Move the rising edge of C1 to the center screen.
5. Set the time/div to 100 ps/div (or faster)
6. Set BWL to 6 GHz (6 GHz and “Full” may be the same when using the D610/D620) in the channel menu.
7. Turn on averaging, set to 50 averages in the channel menu
8. Move the Horizontal position to place C1 edge at center screen. Once this is set for the first probe, do not adjust the Horizontal offset for any channels.
9. Save C1 into M1 and select to display it
10. Disconnect the C1 probe, and connect the C2 probe to PCF200
11. Do not touch the horizontal position control
12. Dial in deskew from the C2 menu align C2 and M1. Use the Deskew measurement parameter: Deskew(M1,C2) to measure accurate skew at the 50% level.
13. Repeat the same steps for C3 (and C4 if using 4 probes)

Post-steps:
1. Set averaging back to 1 on all channels.
2. Set trigger source back to C1.

Note: Skew is negligible through the probe tip. The same tip can be used for all three probes during DDR3 deskew.
Determining DDR Probe / Scope Bandwidth
How To Determining Scope Bandwidth Requirements for DDR Testing:

Step 1. The JEDEC DDR3 Standard Specification JESD79-3F Table 35 lists the DDR3-1600 maximum slew rate as 10 V/ns:

$$
\text{Equation 1: } \text{DDR3 Fastest Risetime} = \frac{\text{Maximum Voltage swing}}{\text{Maximum Slew rate}}
$$

This calculation assumes both worst case voltage swing and worst case slew rate.
Step 2. Convert from slew rate to risetime:

The JEDEC DDR3 Standard Specification JESD79-3F Table 1 lists the DDR3 Vdd supply voltage as 1.5 V. For differential data, the maximum voltage swing is

\[ 2 \times 1.5 \text{ V} = 3.0 \text{ V} \]

**Equation 1**: DDR3 Fastest Risetime

\[ \text{DDR3 Fastest Risetime} = \frac{\text{Maximum Voltage swing}}{\text{Maximum Slew rate}} \]

To compute 20-80% \( T_r \) below, we need to convert the maximum voltage swing (3.0 V) to 20%-80% voltage swing (which is 60% of the total voltage swing):

Maximum voltage swing (20% - 80%) = (60% x 3.0 V) = 1.8 V.

Combining the values from Tables 1 and 35:

\[ \text{DDR3 Fastest Risetime 20-80\% } T_r = \frac{1.8 \text{ V}}{10 \text{ V/ns}} = 180 \text{ ps} \]
To relate measured risetime to the actual (device) risetime and system (oscilloscope + probe) risetime:

**Equation 2:** Measured risetime = $\sqrt{(\text{System risetime})^2 + (\text{Actual risetime})^2}$

The system risetime for each scope + probe combination is listed in the corresponding probe datasheet:

<table>
<thead>
<tr>
<th>D830, D830-PS</th>
<th>Dxx30-SI, Dxx30-SMA-SMP, and Dxx30-PT Tips</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rise Time (20–80%)</td>
<td>37.5 ps (typical)</td>
</tr>
</tbody>
</table>

System rise time measured with $\geq$8 GHz oscilloscope

<table>
<thead>
<tr>
<th>D620, D620-PS</th>
<th>Dx20-SI and Dx20-PT Tips</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rise Time* (20–80%)</td>
<td>56 ps (typical)</td>
</tr>
</tbody>
</table>

*All Bandwidth and Rise Time measurements are made with an oscilloscope bandwidth greater or equal to the probe bandwidth
Equation 2: Measured risetime = \( \sqrt{(\text{System risetime})^2 + (\text{Actual risetime})^2} \)

Using Equation 2, and inserting values from the probe datasheets and the DDR3 JEDEC specification:

Using a 6 GHz probe/scope system for DDR3-1600:

Measured risetime 20-80%: \( \sqrt{(56 \text{ ps})^2 + (180 \text{ ps})^2} = \sqrt{3136 + 32400} = 188.5 \text{ ps} \)

Measurement error = \( \frac{\text{Measured} - \text{Actual}}{\text{Actual}} \frac{188.5 - 180}{180} = 4.7 \% \text{ error} \)

Using an 8 GHz probe/scope system for DDR3-1600:

Measured risetime 20-80%: \( \sqrt{(37.5 \text{ ps})^2 + (180 \text{ ps})^2} = \sqrt{1406.25 + 32400} = 183.9 \text{ ps} \)

Measurement error = \( \frac{\text{Measured} - \text{Actual}}{\text{Actual}} \frac{183.9 - 180}{180} = 2.2 \% \text{ error} \)
Questions?

- Example DDR Test Configurations
- Best Practices for DDR Probing
- DDR Connectivity With An Interposer
- Removing Resistors When Using Interposers
- Connectivity Examples Not Recommended
- Generating DDR Traffic
- DDR Waveform Checklist Before Compliance
- DDR Eye Pattern Formation
- Multiple-Scenario DDR Eye Patterns and Jitter
- Real-World DDR Debug: Missing Clock Cycles
- Real-World DDR Debug: Problem With Read Burst
- Real-World DDR Debug: Logic, Soldering, Power Supply
- DDR Measurement Highlighter
- DDR Virtual Probing
- DDR Compliance Testing
- DDR Specialized Connectivity
- DDR Probe Deskew
- Determining DDR Probe / Scope Bandwidth