Characterization and Jitter Analysis

Digital Signals are Everywhere

- Parallel and serial buses are prevalent
  - Communication among devices within design
  - Communication with outside world
- Many buses, many signals
- Increasing Signal Speeds
- Increasing Signal Integrity Challenges
### Different levels of Embedded System Performance

<table>
<thead>
<tr>
<th>Performance/Design Complexity</th>
<th>Low-Medium</th>
<th>Medium</th>
<th>High</th>
</tr>
</thead>
<tbody>
<tr>
<td>Customer product examples</td>
<td>Appliance, PDA, Camera, GPS</td>
<td>Mobile Phone, Auto, Electric Vehicle, Avionics, Medical Electronics</td>
<td>Network Router, Videogame, Medical Imaging</td>
</tr>
<tr>
<td>Bus or I/O speed (Note: bus is somewhere in the system, e.g. STB with PCIe and SATA)</td>
<td>&lt;300 Mb/s</td>
<td>300 Mb/s – 2.5 Gb/s (DDR2)</td>
<td>&gt;=2.5 Gb/s (&gt;DDR2)</td>
</tr>
<tr>
<td>Adv. acquisition characterization and analysis (e.g. Jitter analysis)</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Multiple stds used or compliance required</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
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### Jitter Basics

**Definitions and Visualization Tools**
Jitter Defined

- **What is jitter?**
  - “The deviation of an edge from where it should be”
  - *ITU Definition of Jitter:* “Short-term variations of the significant instants of a digital signal from their ideal positions in time”

**Why Do We Even Care About Jitter?**

- Simply put, too much jitter causes errors.
Where is the Edge?

- In real life, signals don’t have vertical edges and flat tops / bottoms…

- One or more Reference Levels must be specified before edges can be defined
  - Jitter Correlation is especially sensitive to reference levels

Jitter is caused by many things…

- Thermal noise
  - Generally Gaussian
  - External radiation sources
  - Like background conversations…random and ever changing

- Injected noise (EMI/RFI) & Circuit instabilities
  - Usually a fixed and identifiable source like power supply and oscillators
  - Will often have harmonic content
  - Transients on adjacent traces
  - Cabling or wiring (crosstalk)

- PLL’s problems
  - Loop bandwidth (tracking & overshoot)
  - Deadband (oscillation / hunting)

- Transmission Losses
  - There is no such thing as a perfect conductor
  - Circuit Bandwidth
  - Skin Effect Losses
  - Dielectric Absorption
  - Dispersion – esp. Optical Fiber
  - Reflections, Impedance mismatch, Path discontinuities (connectors)
There are Many Jitter Terms

- Random Jitter (RJ)
- Deterministic Jitter (DJ)
  - Periodic Jitter (PJ)
  - Sinusoidal Jitter (SJ)
  - Duty Cycle Distortion (DCD)
  - Data-Dependent Jitter (DDJ)
  - Inter-Symbol Interference (ISI)
- Total Jitter ~ (TJ or TJ@BER)
- Bit Error Rate (BER)
- Eye Width @BER
  - versus Actual or Observed Eye Width

Random Jitter Defined (RMS)

- Random Jitter (Rj): High frequency timing errors that are not correlated with the data transmitted

- Possible sources:
  - PLL in the data source
  - Noise in the retiming stage of the data source
  - Thermal noise or other random noise effects induced into the phase of the clock or data.

  Rj is Measured in RMS Gaussian Probability Density Function (PDF)
Deterministic Jitter Defined ($P_k - P_k$)

- **Deterministic Jitter** ($D_j$): Timing jitter that is repeatable and predictable.

- **Dj Components:**
  - $P_j/S_j$ – Periodic/Sinusoidal Jitter
  - $Ddj/ISI$ – Data Dependent Jitter / Inter Symbol Interference
  - $DCD$ – Duty Cycle Distortion

- **Possible sources:**
  - Insufficient bandwidth in coupling to optical drive (ac coupled)
  - Overdriving the laser (cutoff or saturation) inducing long recovery time
  - Predictable, Bounded, has definite limits in amplitude

  *Caused by a specific process or component interaction
  $P_k-P_k$ is the method used to specify $Dj$*

Total Jitter

- **Total Jitter** ($T_j$): Total observed jitter (in the form of TIE) broken down into its components, based on known properties of the signal
Jitter Visualization

How can we view and understand Jitter

- Graphical views of jitter provide great insight into jitter behavior
  - Eye Diagram
    - A lot of information in one display
    - Jitter, Noise, Rise time, Overshoot, Duty Cycle, etc.
What is An Eye Diagram?

One Measurement contains a wealth of Information
- Reveals combined transmitter characteristics
- Rise time and Fall time
- Overshoot and Undershoot
- Ringing (Ringback)
- Eye Opening
- Duty Cycle
- Jitter and Noise
- And More…

Eye Diagram Notes
- Larger opening indicates a greater tolerance for noise and jitter
- Larger opening indicates better receiver sensitivity
- Wide top, base and transition region indicates reduced receiver sensitivity
- Eye opening can be correlated with Jitter and BER (JIT3)
Tool of Choice – DPO7000 Series
Powerful and Comprehensive Jitter Analysis

- Assure that the signal acquisition does not significantly contribute to the measured jitter.
  - Up to 3.5 GHz Bandwidth
  - Up to 40GS/s sample rate, 10GS/s/channel
  - >250,000 wfms/s on all channels
  - 100 MPts record length on all channels
  - Highly accurate Probes

- Understanding the cause starts with analysis of captured results
  - Eye Diagram
    - A lot of information in one display
    - Jitter, Noise, Rise time, Overshoot, Duty Cycle, etc.
  - Histogram:
    - Frequency of Occurrence versus Jitter Amplitude
    - To a practiced eye, allows quick assessment of RJ vs. DJ, and how the DJ is distributed
  - Spectrum:
    - Jitter Amplitude versus Frequency
    - Deterministic jitter that is not discernable in other domains is easily seen
    - Root cause can be traced back due to spectral signature
Tool of Choice – DPO7000 Series
Powerful and Comprehensive Jitter Analysis

- Histogram, Spectrum and Numeric Jitter Separation

Tool of Choice – DPO7000 Series
Virtual Demo – One Touch Wizard
Certification and Compliance Tests

Physical Layer Compliance Testing (e.g. USB2.0)

- Embedded Design Challenges
  - Very few designers have the time to be a USB compliance expert
    - Compliance is not the primary consideration – it is a business necessity
    - Number of tests > 10, each requiring different measurement setups

  My manager says we need to pass these tests
  or "marketing" can't put the USB logo on our new product....
USB2.0 Test Requirements

- **USB2.0 Legacy tests**
  - Signal Quality Test (Low and Full Speed)
  - Inrush current test
  - Drop & Droop test
  - Back Voltage (requires a special test fixture – not supported – easy to do)

- **HS Specific tests**
  - Receiver Sensitivity test
  - Chirp test
  - Monotonicity test
  - Impedance Measurement test
  - Hub – System Disconnect Detect (not supported - requires special hub test fixture)
  - Packet Parameter, Resume, Suspend and Reset tests

- **Interoperability**
  - Best performed at a plug fest or with a third party test house

USB2.0 Compliance Test Solution

**TDSUSB2**

- Fully Compliant with USB-IF Tests for USB 2.0 Compliance Testing
  - Automated Setups for Various Tests
  - Automated Eye-diagram Analysis
  - User-configurable Report Formats For Customization

- Comprehensive Test Fixture
  - Enables Quick Setup for a Wide Range of Tests

- In depth analysis
  - Beyond pass/fail results
Debug and Compliance Tools
DPO7000/DSA70000B

- **DPOJET Jitter And Eye Diagram Analysis (opt. DJA)**
  Eye diagram, jitter, and timing analysis for real-time oscilloscopes

- **DDR Memory Bus Analysis (opt. DDRA)**
  DDR1, LP-DDR1, DDR2, DDR3 and GDDR3 read/write qualification, debug and compliance of JEDEC measurements

- **Ethernet Compliance Test Solution (opt. ET3)**
  Full PHY layer support for Ethernet variants 10BASE-T, 100BASE-TX, and 1000BASE-T

- **FB-DIMM Compliance Test Solution (opt. FBD)**
  Receiver, Transmitter and Reference clock compliance test points as per FB-DIMM standards

- **USB2.0 Compliance Test Solution (opt. USB)**
  USB compliance testing including automated probe deskew

- **Ultra Wideband Spectral Analysis Software (opt. UWB)**
  WiMedia PHY Test Spec 1.2 Analysis

...and more